PCI Express® Basics

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Acknowledgements

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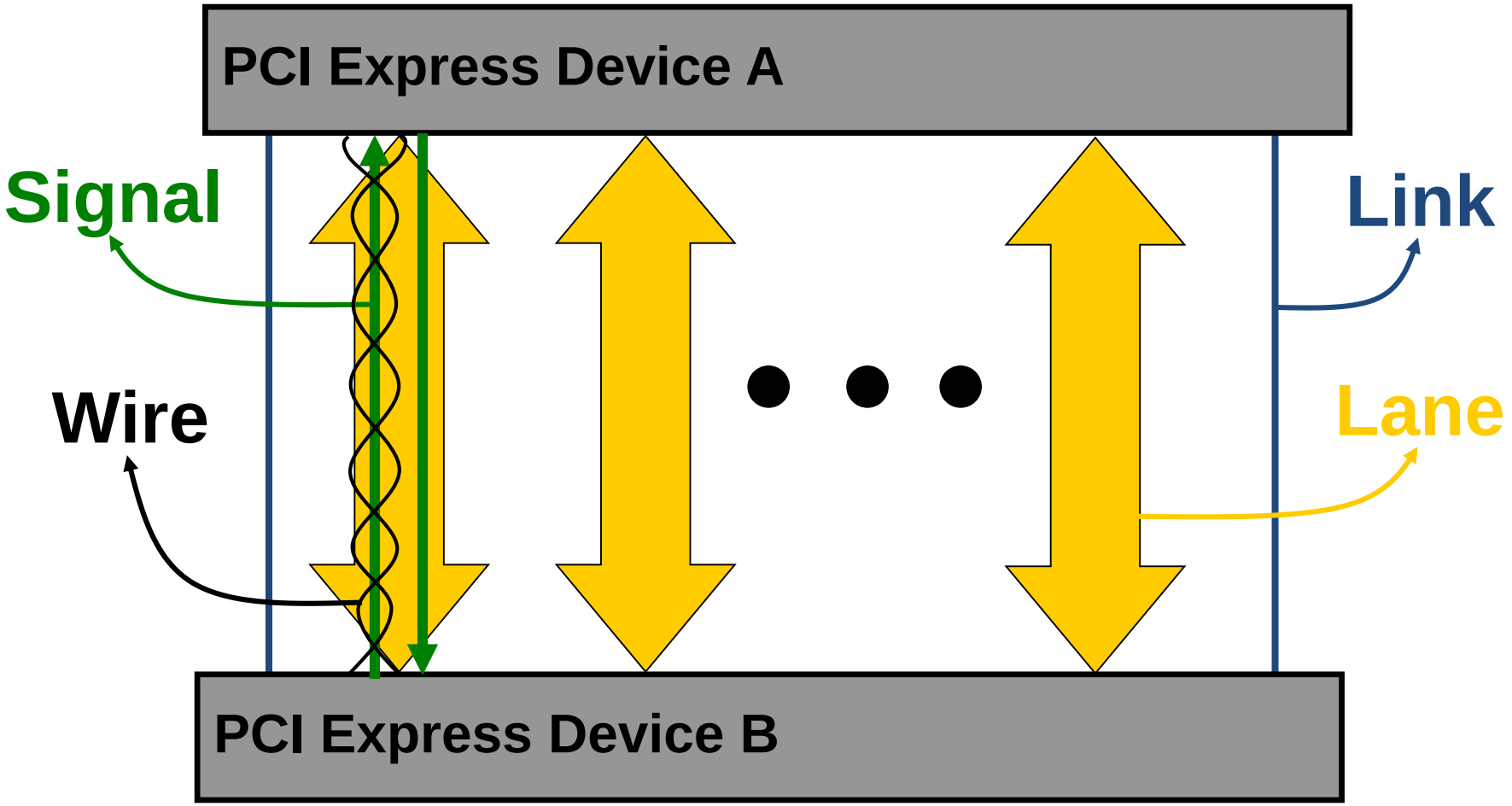
PCI Express® Introduction

- **PCI Express architecture is a high performance, IO interconnect for peripherals in computing/communication platforms**
- **Evolved from PCI™ and PCI-X™ architectures**
  - Yet PCI Express architecture is significantly different from its predecessors PCI and PCI-X
- **PCI Express is a serial point-to-point interconnect between two devices**
- **Implements packet based protocol for information transfer**
- **Scalable performance based on number of signal Lanes implemented on the PCI Express interconnect**

PCI Express Terminology



PCI Express Throughput

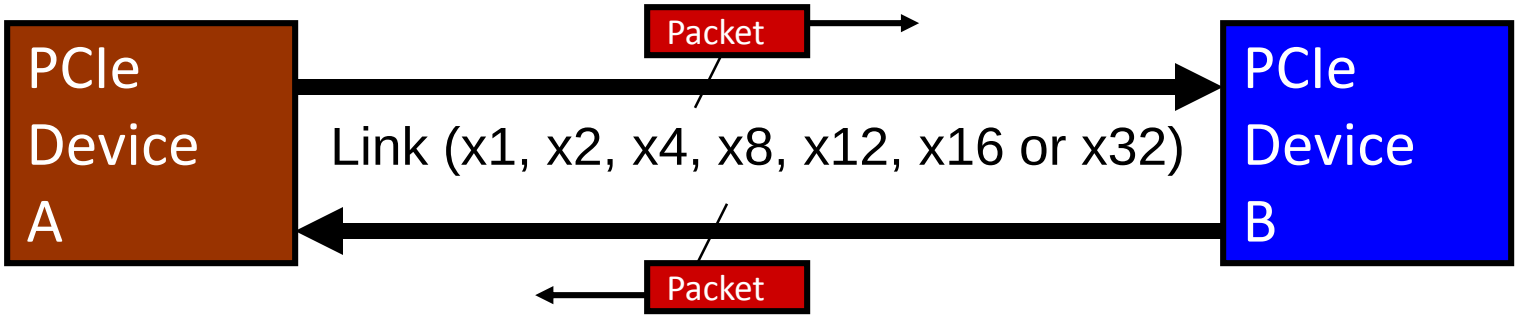
Bandwidth (GB/s)	Link Width				
	x1	x2	x4	x8	x16
PCIe® 1.x "2.5 GT/s"	0.25	0.5	1	2	4
PCIe 2.x "5 GT/s"	0.5	1	2	4	8
PCIe 3.0 "8 GT/s"	1	2	4	8	16
PCIe 4.0 "16GT/s"	*2*	*4*	*8*	*16*	*32*

Derivation of these numbers:

- **20% overhead due to 8b/10b encoding in 1.x and 2.x**
- **Note: ~1.5% overhead due to 128/130 encoding not reflected above in 3.x and 4.0**

PCI Express Features

- **Dual Simplex point-to-point serial connection**
  - Independent transmit and receive sides
- **Scalable Link Widths**
  - x1, x2, x4, x8, *x12*, x16, *x32*
- **Scalable Link Speeds**
  - 2.5, 5.0 and 8.0GT/s (16GT/s coming in 4.0)
- **Packet based transaction protocol**



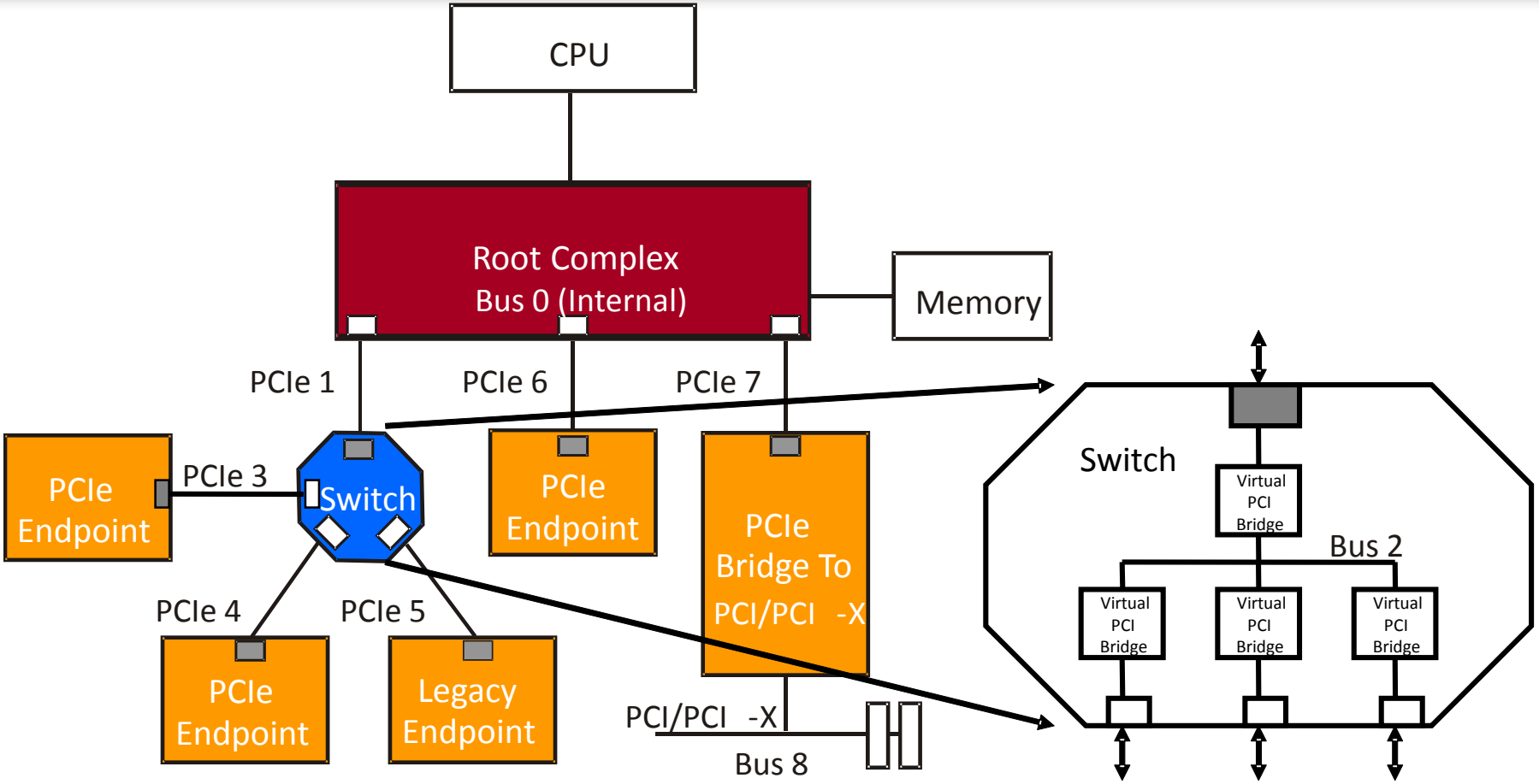
Additional Features

- **Data Integrity and Error Handling**
  - Link-level “LCRC”
  - Link-level “ACK/NAK”
  - End-to-end “ECRC”
- **Credit-based Flow Control**
  - No retry as in PCI
- **MSI/MSI-X style interrupt handling**
  - Also supports legacy PCI interrupt handling in-band
- **Advanced power management**
  - Active State PM
  - PCI compatible PM

Additional Features

- **Evolutionary PCI-compatible software model**
  - PCI configuration and enumeration software can be used to enumerate PCI Express hardware
  - PCI Express system will boot “PCI” OS
  - PCI Express supports “PCI” device drivers
  - New additional configuration address space requires OS and driver update
    - Advanced Error Reporting (AER)
    - PCI Express Link Controls

PCI Express Topology



Legend

PCI Express Device Downstream Port

PCI Express Device Upstream Port

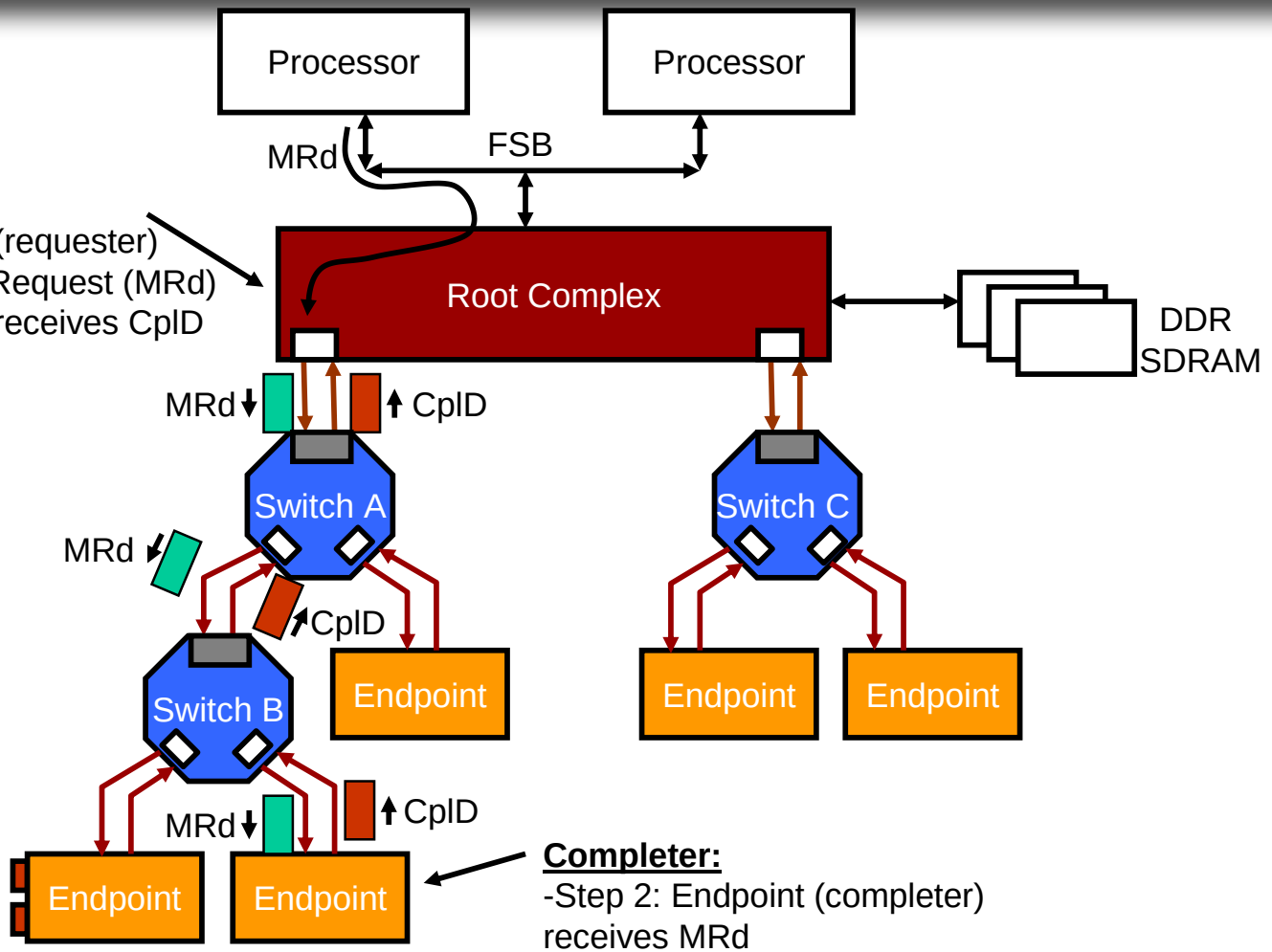
Transaction Types, Address Spaces

- **Request are translated to one of four transaction types by the Transaction Layer:**
  1. **Memory Read or Memory Write**. Used to transfer data from or to a memory mapped location.
     - The protocol also supports a *locked memory read* transaction variant
  2. **I/O Read or I/O Write.** Used to transfer data from or to an I/O location.
     - These transactions are restricted to supporting legacy endpoint devices
  3. **Configuration Read or Configuration Write**. Used to discover device capabilities, program features, and check status in the 4KB PCI Express configuration space.
  4. **Messages.** Handled like posted writes. Used for event signaling and general purpose messaging.

Three Methods For Packet Routing

- **Each request or completion header is tagged as to its *type*, and each of the packet types is routed based on one of three schemes:**
  - Address Routing
  - ID Routing
  - Implicit Routing
- **Memory and IO requests use address routing**
- **Completions and Configuration cycles use ID routing**
- **Message requests have selectable routing based on a 3-bit code in the message routing sub-field of the header type field**

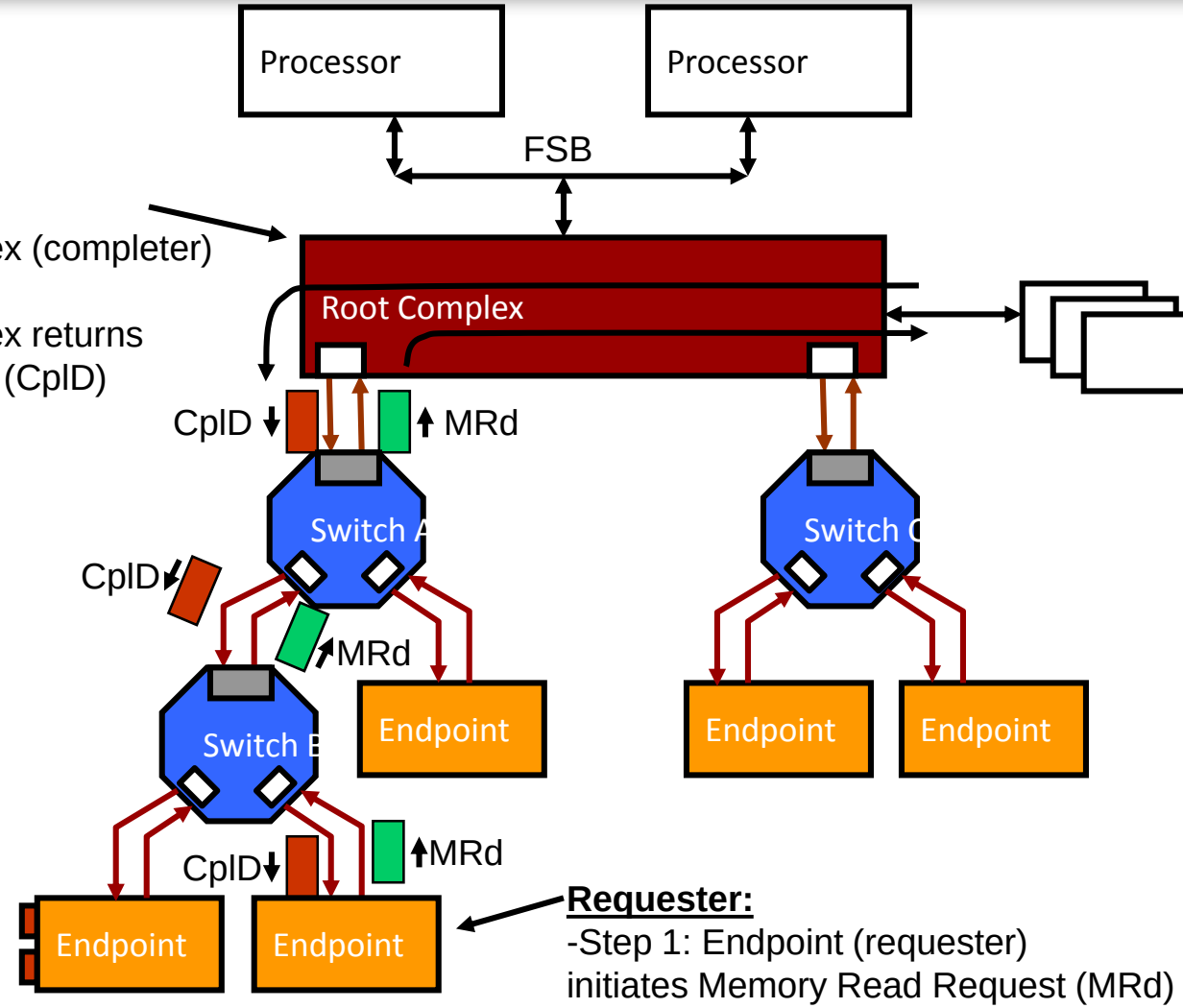
Programmed I/O Transaction



Requester:
-Step 1: Root Complex (requester) initiates Memory Read Request (MRd)
-Step 4: Root Complex receives CplD

Completer:
-Step 2: Endpoint (completer) receives MRd
-Step 3: Endpoint returns Completion with data (CplD)

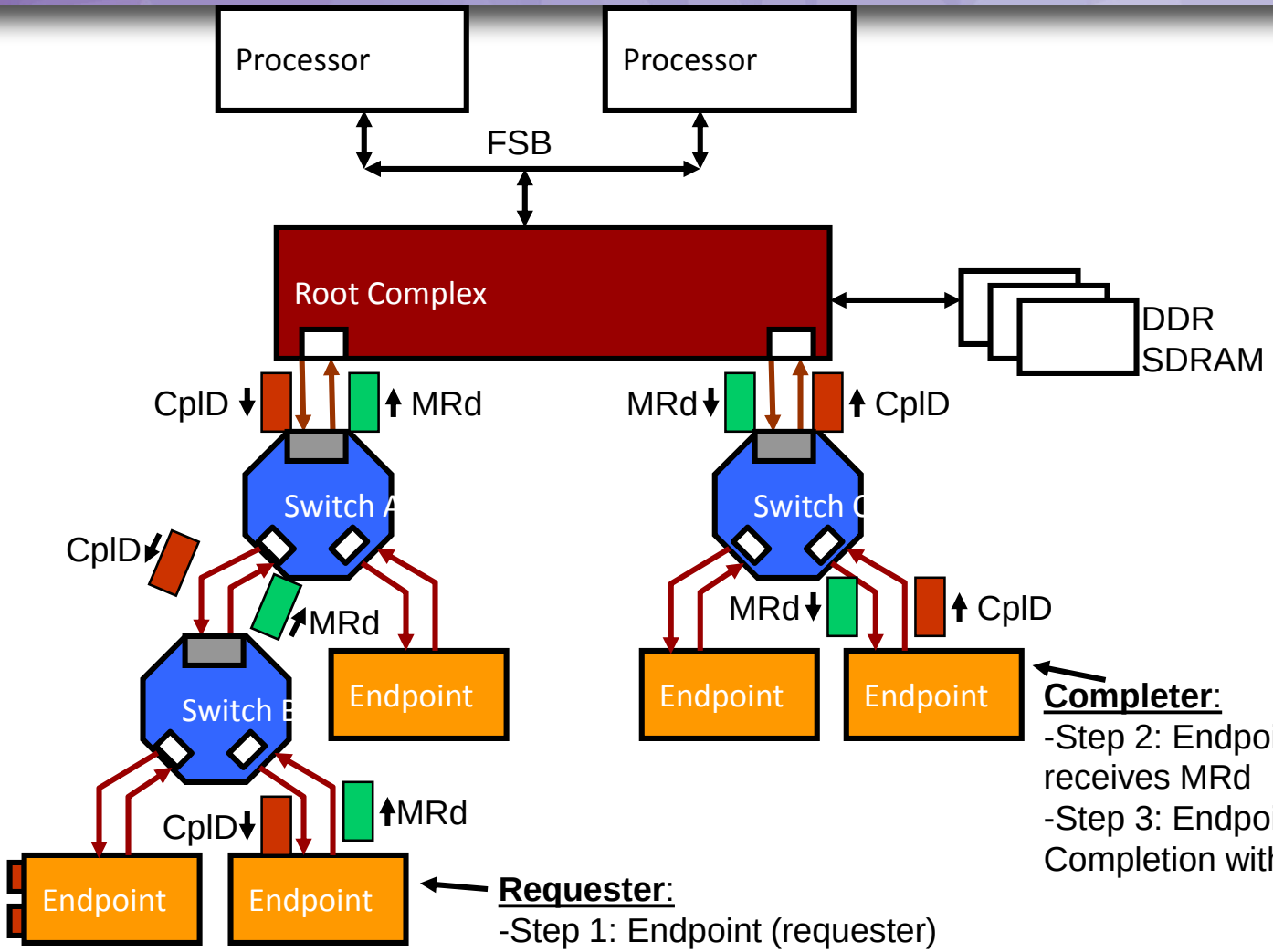
DMA Transaction



Completer:
-Step 2: Root Complex (completer) receives MRd
-Step 3: Root Complex returns Completion with data (CplD)

Requester:
-Step 1: Endpoint (requester) initiates Memory Read Request (MRd)
-Step 4: Endpoint receives CplD

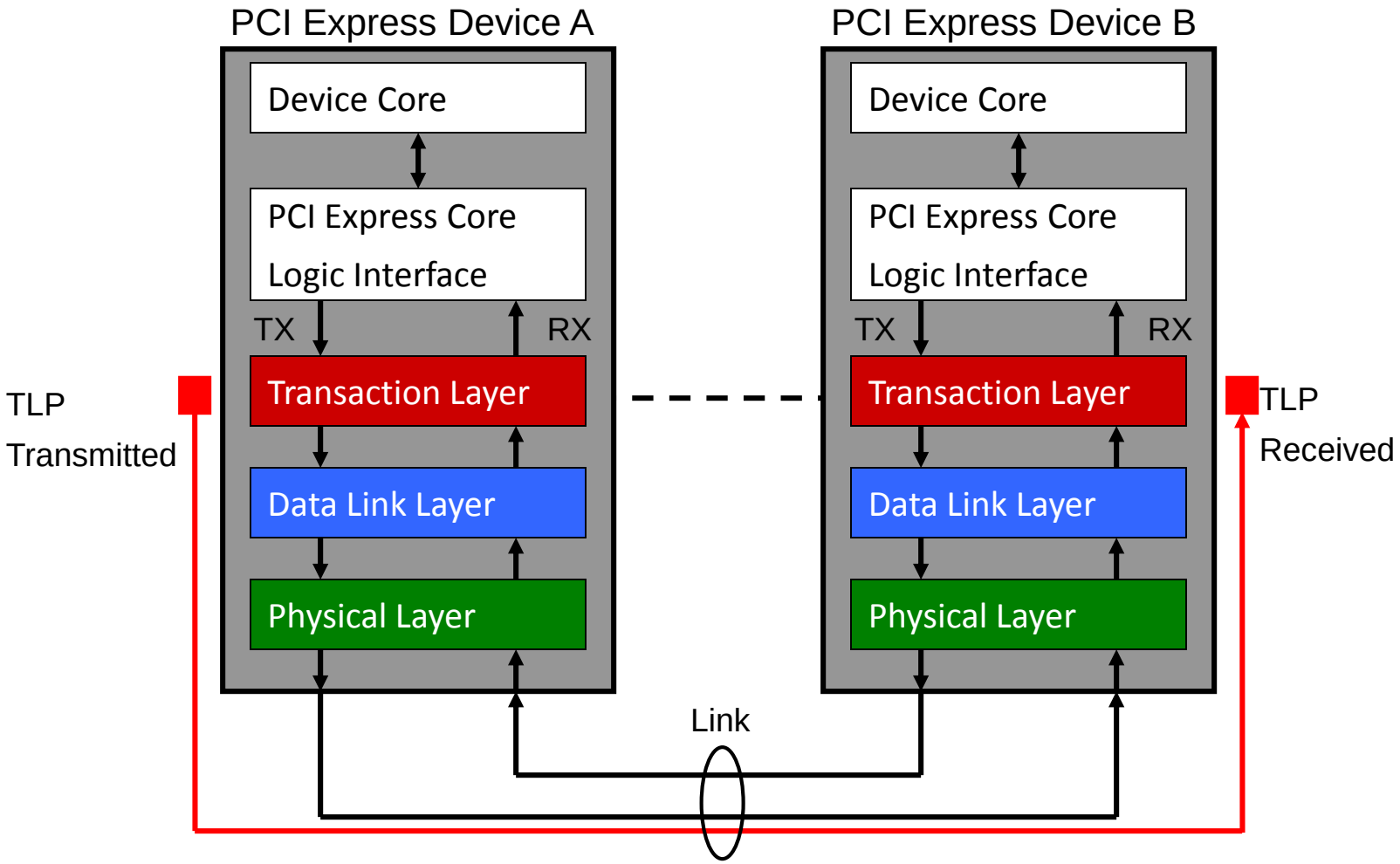
Peer-to-Peer Transaction



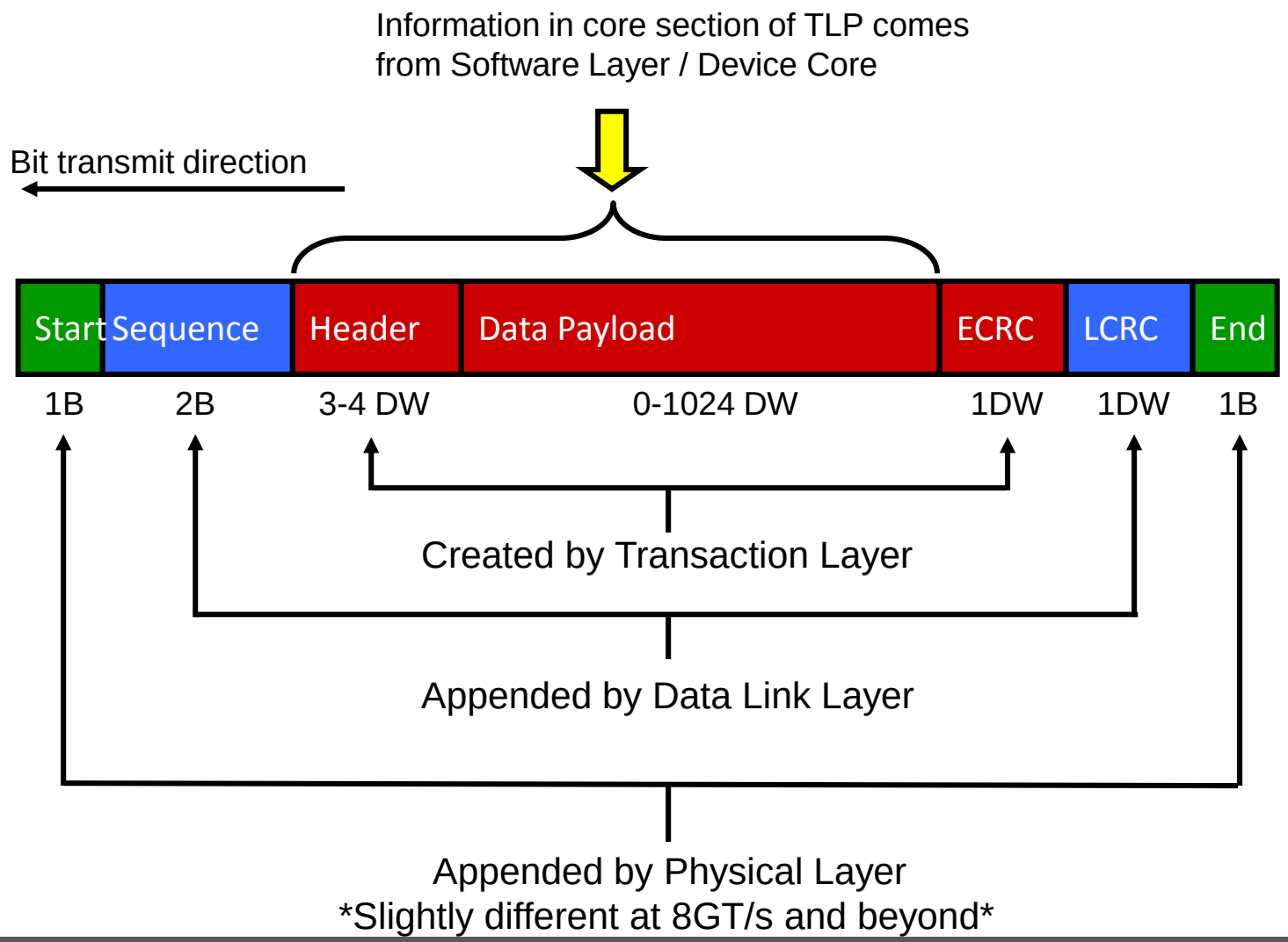
Completer:
-Step 2: Endpoint (completer) receives MRd
-Step 3: Endpoint returns Completion with data (CplD)

Requester:
-Step 1: Endpoint (requester) initiates Memory Read Request (MRd)
-Step 4: Endpoint receives CplD

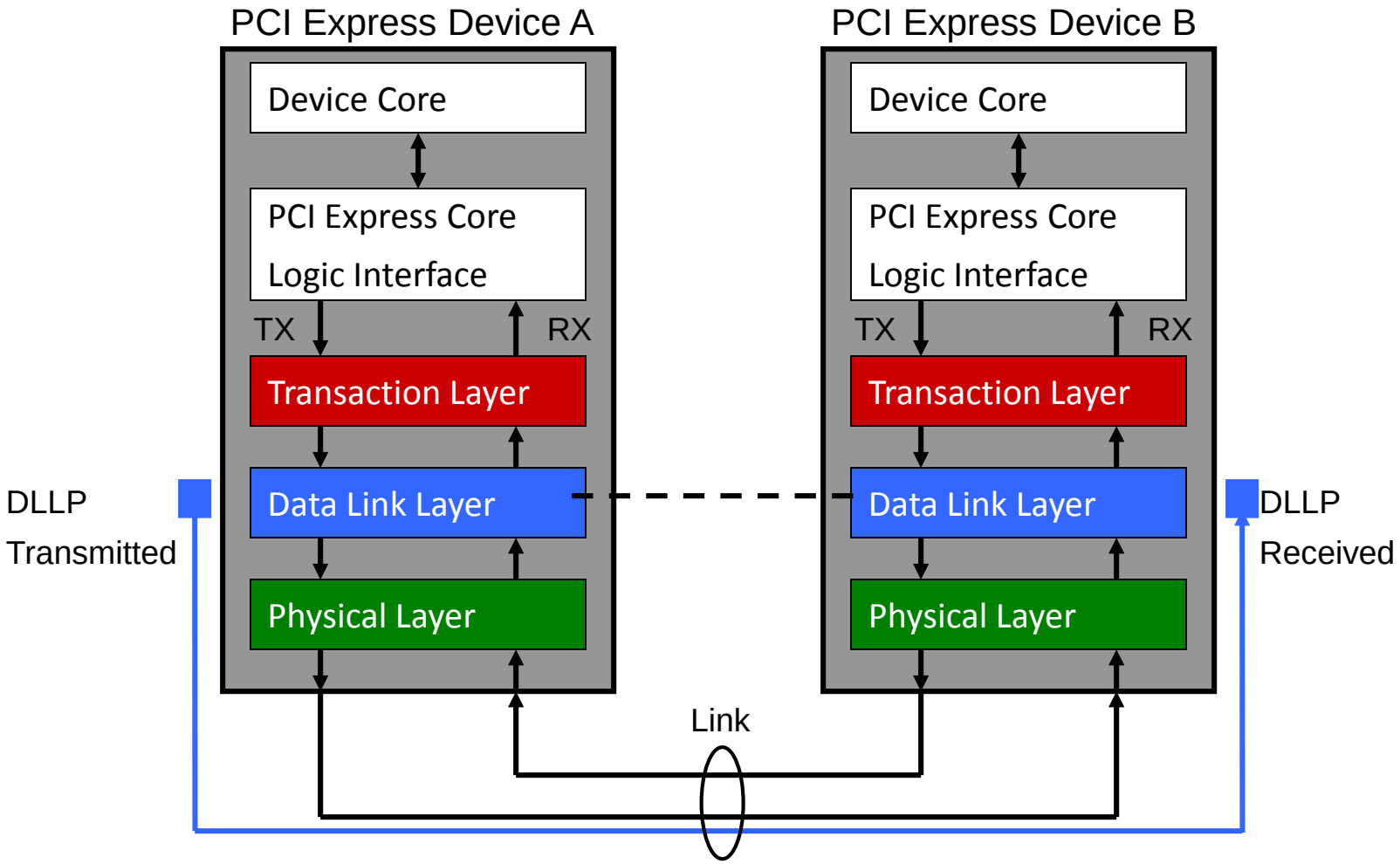
TLP Origin and Destination



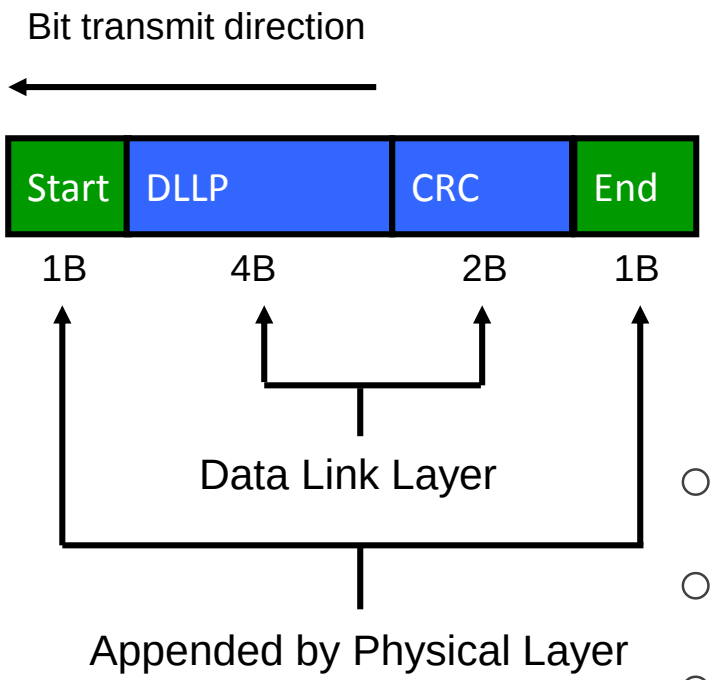
TLP Structure



DLLP Origin and Destination

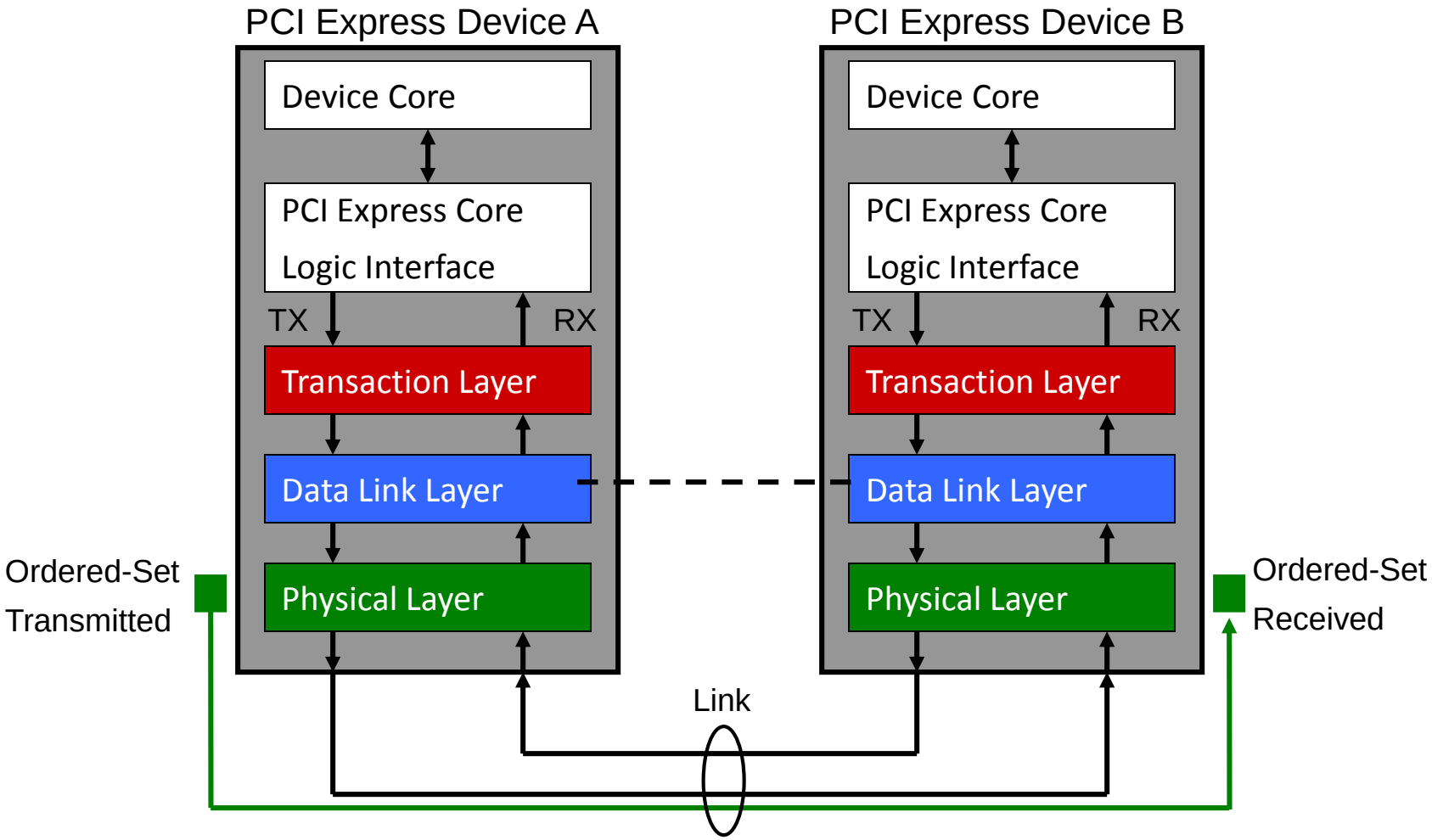


DLLP Structure



- **ACK / NAK Packets**
- **Flow Control Packets**
- **Power Management Packets**
- **Vendor Defined Packets**

Ordered-Set Origin and Destination

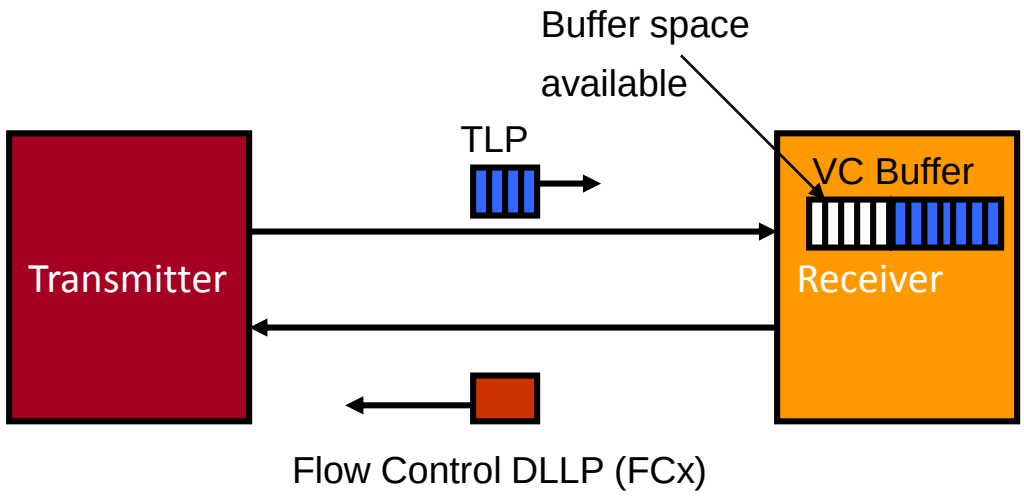


Ordered-Set Structure

- **Training Sequence One (TS1)**
  - 16 character set: 1 COM, 15 TS1 data characters
- **Training Sequence Two (TS2)**
  - 16 character set: 1 COM, 15 TS2 data characters
- **SKIP**
  - 4 character set: 1 COM followed by 3 SKP identifiers
- **Fast Training Sequence (FTS)**
  - 4 characters: 1 COM followed by 3 FTS identifiers
- **Electrical Idle (IDLE)**
  - 4 characters: 1 COM followed by 3 IDL identifiers
- **Electrical Idle Exit (EIEOS) (new to 2.0 spec)**
  - 16 characters

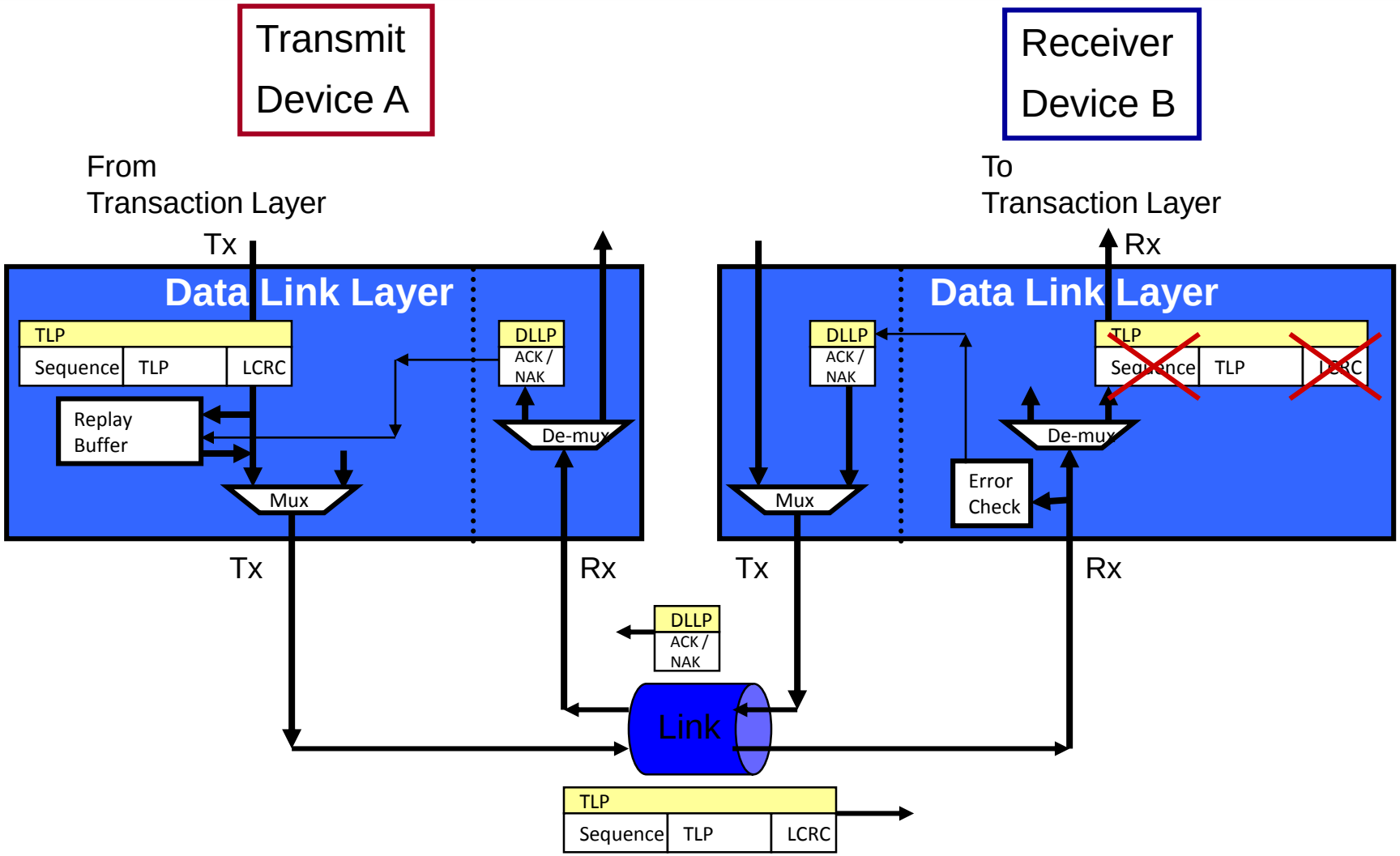
PCI Express Flow Control

Credit-based *flow control* is point-to-point based, not end-to-end



Receiver sends Flow Control Packets (FCP) which are a type of DLLP (Data Link Layer Packet) to provide the transmitter with credits so that it can transmit packets to the receiver

ACK/NAK Protocol Overview



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- **Watch for e-mailed Call For Papers**
- **Send in an abstract!**
  - 160 word summary
    - Ok to attach more detail (even a presentation)
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  - Not a datasheet or catalog or other marketing!
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- **Meet milestones and deadlines**
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